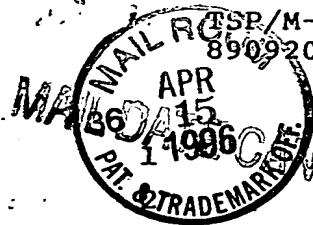


TSP/M-1007
890920 (AHM:)FIELD PROGRAMMABLE PRINTED CIRCUIT BOARD

Amr. M. Mohsen

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FIELD OF THE INVENTION

This invention relates to printed circuit boards and in particular to a printed circuit board which is programmable in the field by the designer of an electronic system to provide a desired function and to the method of programming the programmable printed circuit board of this invention.

BACKGROUND OF THE INVENTION

Printed circuit boards are commonly used in electronic devices such as instruments, computers, telecommunication equipment and consumer electronic products. Typically, an engineer will design a printed circuit board to carry the types of components necessary to implement the desired electronic function and to fit in the space available for the board. Consequently, each printed circuit board typically is custom designed. To design a custom printed circuit board is expensive, takes time and requires the fabrication of prototype printed circuit boards. If errors are found in the prototypes, then the printed circuit board must be redesigned. Such a process often delays the planned introduction of a new product.

SUMMARY OF THE INVENTION

In accordance with this invention, a printed circuit board of unique configuration is combined with one or more special programmable integrated circuit chips (hereinafter called "programmable interconnect chips" or "PICs") to provide a user programmable printed circuit board capable of being used to provide any one of a plurality of functions.

In one embodiment of the invention, a field programmable printed circuit board comprises

- (1) a multiplicity of component contacts for receipt of the leads of electronic components;
- (2) a corresponding multiplicity of PIC contacts

1 for receipt of the leads on the package or packages of
2 the programmable interconnect chip or chips; and

3 (3) one or more layers of conductive traces, each
4 conductive trace uniquely connecting one component
5 contact to one PIC contact.

6 Typically, electronic components comprise integrated
7 circuits and/or discrete devices contained, respectively, in
8 standard integrated circuit or discrete device packages and
9 in addition, discrete elements which include resistors,
10 capacitors and inductors, for example.

11 Generally the component contacts and PIC contacts
12 comprise holes in the printed circuit board, the interior
13 surfaces of which are plated to a selected thickness with a
14 conductive material such as copper. Alternatively, these
15 contacts are pads or any other structure for electrically
16 and physically joining electronic components and integrated
17 circuits to a printed circuit board. Advantageously, the
18 PIC contacts are usually (though not necessarily) smaller
19 than the component contacts so that the area of the
20 programmable printed circuit board occupied by the
21 programmable interconnect chip or chips is much smaller than
22 the area of the printed circuit board occupied by the
23 electronic components. Each PIC contact brings a
24 corresponding trace from a selected level on the PC board to
25 the surface of the PC board so that trace is then
26 connectable to a pin or electrical contact on a programmable
27 interconnect chip. For every component contact (the
28 function of which is to receive the pin or electrical
29 contact of an electronic component) there is a corresponding
30 electrically conductive trace which interconnects that
31 component contact to a corresponding PIC contact (the
32 function of which is to receive the pin or electrical
33 contact of the programmable interconnect chip) in the
34 printed circuit board. Thus, each component contact is
35 electrically and uniquely connected to a corresponding PIC
36 contact for electrically contacting a programmable
interconnect chip of this invention.

37 In accordance with this invention more than one
38

1 programmable interconnect chip is, if desired, placed on a
2 printed circuit board to provide enhanced interconnection
3 flexibility and cost optimization for the electronic
4 components on the printed circuit board. Such a board then
5 has additional PIC contacts corresponding to and for
6 connection to the external pins or electrical contacts on
7 the additional packages containing the additional
8 programmable interconnect chips.

9 The field programmable printed circuit board
10 (hereinafter sometimes referred to as a "FPPCB") of this
11 invention substantially reduces the cost associated with
12 developing complex electronic systems by providing a
13 standard PC board configuration which is easily and
14 economically manufactured. In accordance with this
15 invention, the designer of electronic systems utilizing the
16 standard programmable PC board of this invention will also
17 utilize computer aided design software to determine the
18 optimum placement of the electronic components on the
19 programmable PC board and to determine the configuration of
20 the programmable interconnect chip or chips of this
21 invention to properly interconnect the electronic components
22 so as to yield the desired electronic system.

23 In accordance with the method of this invention a user
24 designing an electronic system utilizing the programmable
25 PC board of this invention will first place a model of the
26 programmable PC board in the computer aided design system.
27 The user then will simulate the placement of models of the
28 desired electronic components, be they discrete elements,
29 memory, logic gates, or microprocessors, on selected
30 component contacts on the programmable PC board and will
31 simulate the interconnection of these electronic components
32 using the standard PC board of this invention together with
33 the programmable interconnect chip or chips of this
34 invention. The computer will then simulate the electrical
35 performance of the system with the electrical components so
36 placed and interconnected and will indicate whether or not
37 the configuration selected by the designer yields the
38 desired electronic function. The designer will have choices

1 in the placement of the electronic components on the
2 programmable PC board and in their interconnection but will
3 be assisted in this placement by certain logical rules
4 contained in the computer aided design program. Algorithms
5 for use in computer aided design systems of the type
6 required to implement the design of electronic systems
7 utilizing the programmable PC board and programmable
8 interconnect chip of this invention are of a type currently
9 available in the electronic design industry.

10 The programmable printed circuit board of this
11 invention is considered to be "field programmable" because
12 the designer of an electronic system is able to program the
13 placement of electronic components on the unique PC board of
14 this invention by using and configuring the programmable
15 interconnect chips of this invention. The PC board of this
16 invention is unique in that it has a standard configuration
17 regardless of the electronic function to be implemented and
18 thus is relatively inexpensive and easy to make. At the
19 same time, the field programmable PC board of this invention
20 is programmable by use of one or more programmable
21 interconnect chips.

22 In an alternative embodiment of this invention, the
23 programmable PC board of this invention includes on a
24 portion of its surface electronic components which are
25 interconnected using custom designed interconnections to
26 form a particular circuit function. Conductive traces
27 transmit the signals from this custom portion of the PC
28 board to one or more programmable interconnect chips on the
29 remainder of the PC board. The programmable interconnect
30 chip or chips are configured by the user to achieve the
31 desired function required utilizing both the custom portion
32 of the PC board and the programmable portion of the PC
33 board.

34 Throughout this specification, the field programmable
35 PC board of this invention will usually be described as
36 having component holes and PIC holes for receipt of the
37 electrical leads of the electronic components and of the
38 programmable interconnect chip, respectively. The term

1 "component hole" and the term "PIC hole" will be used to
2 describe a standard hole formed in a PC board and plated
3 with a conductive material as in the prior art to receive a
4 conductive lead. However, any conductive structure capable
5 of being used to electrically contact and physically hold
6 the package of an electronic component can be used in place
7 of a component hole or a PIC hole. Such a structure
8 includes a solder pad and a socketed printed circuit board
9 opening for slidably receiving and releasing the pins of an
10 electronic component package. It should be noted that the
11 term PIC hole is used to distinguish the function of certain
12 holes in the programmable printed circuit board of this
13 invention from the component holes. However, both types of
14 holes are plated with a conductive material and have the
15 same purpose -- that is to electrically transmit signals
16 from either the pin of the package of an electronic
17 component to a conductive trace or from a conductive trace
18 to the pin of an electronic component or through the
19 programmable interconnect chip to another trace or from a
20 conductive trace to another conductive trace.

21 In certain circumstances, a PIC hole or a component
22 hole can be used to interconnect two traces directly. Such
23 a configuration occurs in custom designed PC boards.

24 This invention will be more fully understood in
25 conjunction with the following detailed description together
26 with the attached drawings.

27
28 DESCRIPTION OF THE DRAWINGS

29 Figure 1a illustrates in isometric view a programmable
30 printed circuit board of this invention containing a
31 plurality of layers of traces such as trace 103-r,c each
32 trace connecting uniquely one component hole 102-r,c to a
33 corresponding PIC hole 104-r,c (shown in Figure 1b);

34 Figure 1b illustrates an isometric view of the portion
35 of the programmable PC board 100 of Figure 1a beneath
36 programmable interconnect chip 105 containing the PIC holes
37 (such as hole 104-r,c) for connection of the traces (such as
38 trace 103-r,c) to the pins or electrical contacts on the

1 programmable interconnect chip 105 of this invention;

2 Figures 2a through 2d illustrate schematically four top
3 plan views of printed circuit board 100 utilizing the
4 programmable interconnect chip 105 of this invention
5 together with the multiplicity of component holes 102-1,1
6 through 102-R,C (not shown) arranged on the printed circuit
7 board together with a schematic representation of conductive
8 busses 103 each bus containing a plurality of conductive
9 traces such as traces 103-1,1 through 103-1,3 for
10 interconnecting each of the component holes 102 to a
11 corresponding PIC hole 104 beneath the programmable
12 interconnect chip 105;

13 Figures 3a, 3b, 3c and 3d illustrate a number of
14 different global interconnect architectures suitable for use
15 with this invention;

16 Figures ~~4a and 4b~~ ^{4a-4c} illustrate respectively the top and
17 side views of a programmable printed circuit board 400
18 constructed in accordance with this invention together with
19 a programmable interconnect chip 405 placed on the board to
20 interconnect the electronic components to be placed on the
21 PC board 400 in a selected manner to provide the desired
22 electronic function;

23 Figure 5 illustrates a programmable printed circuit
24 board 500 of this invention containing a test ^{port} and a
25 control port for testing the state of each trace on the
26 programmable printed circuit board 500 and for configuring
27 the programmable interconnect chip 505 to interconnect in
28 the desired manner the electronic components 506-1 through
29 506-4 placed on the PC board 500;

30 Figures 6a through 6e illustrate a number of structures
31 for implementing the programmable interconnect chip 605
32 suitable for use in implementing the programmable PC board
33 of this invention;

34 Figure 7a illustrates the architecture of the
35 programmable interconnect chip 605;

36 Figure 7b illustrates one structure for programming the
37 intersection of two conductive leads formed on the
38 programmable interconnect chip 605;

Figure 7c illustrates a bilateral circuit for controlling the transmittal of signals to or from a test port used in conjunction with the programmable interconnect chip 605 of this invention; and

Figures 8a and 8b illustrate structures for connecting electronic component packages and/or a package containing a programmable interconnect chip to the programmable printed circuit board of this invention. *na²*

DETAILED DESCRIPTION

The following description is meant to be illustrative only and not limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of this description.

Figure 1a is an isometric cross-sectional view of the programmable printed circuit board of this invention. As shown in Figure 1a, programmable PC board 100 comprises a plurality of layers 101-1 through 101-4 of insulating material. On each layer 101-i (where $1 \leq i \leq 4$) is formed a plurality of electrical traces 103. Formed in the printed circuit board are a multiplicity of component holes 102-1,1 through 102-R,C where R represents the number of component rows of holes formed on the programmable printed circuit board and C represents the number of columns of component holes formed on the board. Thus, the programmable printed circuit board illustrated in Figure 1a has rows of component holes 102-1,X through 102-R,X (where X is an integer which varies from 1 to C) and has columns of component holes 102-Y,1 through 102-Y,C where Y is an integer which varies from 1 to R. As shown in Figure 1a, traces 103-1,1 through 103-1,C, 103-2,1 through 103-2,C and 103-3,1 through 103-3,C are formed on the top surface of insulating layer 101-1. Traces 103-4,1 through 103-6,C (not shown) are formed on the top surface of layer 101-2. Traces 103-7,1, through 103-9,C (not shown) are formed on the top surface of layer 101-3 and traces 103-10,1 through 103-12,C are formed on the top surface of layer 101-4. Each trace 103-r,c (where r indicates the row and is given by $1 \leq r \leq R$ and c indicates

1 the column and is given by $1 \leq c \leq C$) interconnects a
2 corresponding component hole 102-r,c to a corresponding PIC
3 hole 104-r,c (shown in Figure 1b) connectable to a selected
4 pin on programmable interconnect chip 105 (shown in Figure
5 1a).

6 In the description of Figure 1a, for simplicity not all
7 component holes 102-r,c are actually numbered nor are all
8 traces 103-r,c numbered. However, the numbering the
9 component holes 102-r,c, traces 103-r,c and the PIC holes
10 104-r,c is consistent with each electrically connected
11 component hole 102-r,c, trace 103-r,c and PIC hole 104-r,c
12 all having the same indicia r,c.

13 Figure 1b illustrates PIC hole 104-r,c connected to
14 trace 103-r,c so as to bring the electrical signal on trace
15 103-r,c to the top surface of layer 101-4 of the PC board
16 100 for electrical contact to the programmable interconnect
17 chip (shown in Figure 1a but not in Figure 1b) of this
18 invention. Figure 1b shows an isometric cutaway drawing of
19 a portion of the programmable printed circuit board 100 of
20 this invention with PIC holes 104-1,1 through 104-R,C (not
21 shown) being arranged in a selected location on the printed
22 circuit board 100 so as to bring to a portion of the top
23 surface of insulating layer 101-4 of the printed circuit
24 board 100 the electrical signals carried by traces 103-1,1
25 through 103-R,C. The PIC holes 104-1,1 through 104-R,C
26 (each of which is plated on its interior surface with a
27 conductive material) are arranged in a pattern on the
28 printed circuit board so as to mate with the pins or other
29 electrical connections on the package containing the
30 programmable interconnect chip. Thus the area of the
31 programmable PC board 100 occupied by PIC holes 104-1,1
32 through 104-R,C is desirably (though not necessarily) much
33 smaller than the area of the printed circuit board occupied
34 by component holes 102-1,1 through 102-R,C. The internal
35 diameter of the PIC holes 104-1,1 to 104-R,C is much smaller
36 than the internal diameter of the component holes 102-1,1 to
37 102-R,C and is only sufficient to allow the pins or other
38 electrical connectors on the package of the programmable

1 interconnect chip to make proper electrical contact to
2 traces 103-1,1 through 103-R,C.

3 Figure 2a illustrates in top view the local
4 interconnect architecture of the programmable interconnect
5 chip 105 mounted on the programmable printed circuit board
6 100 of this invention to show the conductive paths followed
7 by the traces 103 interconnecting the component holes 102 to
8 the PIC holes 104. Figure 2a illustrates the conductive
9 traces on one layer 101-1 of PC board 100 only. Each layer
10 of PC board 100 will have a similar pattern of traces. The
11 regions under programmable interconnect chip 105 to which
12 the traces are directed differ from level to level because
13 each trace 103-r,c uniquely interconnects one component hole
14 102-r,c to a corresponding PIC hole 104-r,c. Figure 2b is
15 similar to Figure 2a except it illustrates schematically the
16 trace interconnect structure to interconnect component holes
17 102-r,c to PIC holes 104-r,c utilizing the traces 103-r,c on
18 printed circuit board insulating layer 101-2. Note that the
19 traces 103 on insulating layer 101-2 interconnect different
20 component holes 102^{and PIC holes 104} than do the traces shown in Figure 2a.
21 Similar drawings for the interconnect traces formed on
22 insulating layers 101-3 and 101-4 are shown in Figures 2c
23 and 2d illustrating the different component holes 102-r,c
24 being connected to the PIC holes 104-r,c by the traces 103-
25 r,c on the layers of insulation 101-3 and 101-4.

26 While Figures 2a through 2d illustrate a programmable
27 printed circuit board 100 utilizing one programmable
28 interconnect chip 105 of this invention, more than one
29 programmable interconnect chip 105 can be used with a
30 printed circuit board 105 if desired. The printed circuit
31 board 100 must be configured to provide a plurality of PIC
32 holes 104 beneath each of the programmable interconnect
33 chips 105 utilized on the PC board 100. But with this
34 change the structure of this invention can be made even more
35 flexible and versatile than is possible with just one
36 programmable interconnect chip 105.

37 As shown in Figure 3a a plurality of programmable
38 interconnect chips 301-1 through 301-7 are utilized on PPCB

1 300. Typically, programmable PC board 300 is a multilayer
2 PC board although in certain simple configurations a single
3 layer programmable PC board can be used. Each chip 301-j
4 (where j is an integer represented by $1 \leq j \leq J$) comprises a
5 local programmable interconnect chip. A selected number of
6 pins on chip 301-j are designated to electrically connect to
7 the conductive traces in a bus formed on the programmable PC
8 board 300 to interconnect that programmable interconnect
9 chip 301-j to an adjacent programmable interconnect chip 301
10 such as chip 301-(j+1). Thus, in Figure 3a, programmable
11 interconnect chip 301-1 is capable of interconnecting any
12 one of a plurality of electronic components (not shown)
13 mounted on PC board 300 adjacent to PIC 300-1 with another
14 of that plurality of electronic components. In addition,
15 programmable interconnect chip 301-1 is also able to connect
16 these electronic components by means of buses 303-1 and/or
17 303-5 to the electronic components connected to adjacent
18 programmable interconnect chips 301-2 and 301-5,
19 respectively. Typically, busses 303-1 and 303-5 contain
20 eight communication channels (i.e. eight traces) or 16
21 communication channels or data paths (i.e., 16 traces). Of
22 course, these data busses can contain any number of
23 transmission channels desired depending upon the
24 requirements of the circuitry. The particular data busses
25 303-1 and 303-5 are formed by means of conductive traces
26 formed on a selected surface of PC board 300. Similarly,
27 programmable interconnect chip 301-2 is connectable to
28 programmable interconnect chip 301-3 and 303-4 by means of
29 conductive busses 303-2 and 303-4, respectively. Conductive
30 busses 303-2 and 303-4 have the same characteristics as
31 conductive busses 303-1 and 303-5 previously described and
32 thus will not be described in detail. Likewise, conductive
33 busses 303-3, 303-6, 303-7 and 303-8 interconnect ^{selected} ~~selective~~
34 programmable interconnect chips. Thus, conductive bus 303-3
35 interconnects programmable interconnect chip 301-3 to
36 programmable interconnect chip 301-7. Conductive bus 303-7
37 interconnects programmable interconnect chip 301-4 to
38 programmable interconnect chip 301-6. Conductive bus 303-6

a
1 interconnects programmable interconnect chip 301-5 to
2 programmable interconnect chip 301-6 and conductive bus
3 303-8 interconnects programmable interconnect chip 301-6 to
4 programmable interconnect chip 301-7. Conductive busses
5 303-3 and 303-6 through 303-8 each have the same
6 characteristics as described above in conjunction with
7 conductive busses 303-1 and 303-5 and thus this description
8 will not be repeated. The structure of Figure 3a allows any
9 electronic components on the PPCB to be interconnected with
10 any other electronic component on the PPCB through one or
11 more PIC's.

12 Figure 3b illustrates a second type of interconnect
13 system wherein programmable interconnect chips 311-1, 311-2,
14 311-3, and 311-4 are interconnected by means of conductive
15 busses 313-1 through 313-6. Thus, each programmable
16 interconnect chip 311-1 through 311-4 shown in Figure 3b is
17 connected directly to an adjacent programmable interconnect
18 chip 311 by means of a dedicated conductive bus 313. For
19 example, programmable interconnect chip 311-1 can be
20 connected directly to programmable interconnect chips 311-2,
21 311-3 or 311-4 by means of conductive busses 313-1, 313-5 or
22 313-4, respectively. Each of these conductive busses
23 contains a selected number of conductive lines (such as 8 or
24 16 conductive lines) implemented by means of 8 or 16 traces
25 formed on a particular surface of programmable interconnect
26 chip 300. Similarly, conductive busses 313-6, 313-2 and
27 313-3 have 8 or 16 conductive paths represented by traces
28 formed on the PC board 300 and interconnect pairs of the
29 programmable interconnect chips as shown in Figure 3b. The
30 advantage of the structure shown in Figure 3b over the
31 structure shown in Figure 3a is that each programmable
32 interconnect chip 311 is able to communicate directly to
33 each of the other programmable interconnect chips 311 on the
34 printed circuit board 300. Of course, each programmable
35 interconnect chip 311 also interconnects a plurality of
36 electrical components such as integrated circuits or
37 discrete devices inserted into the programmable PC board in
38 the area adjacent to the programmable interconnect chip

1 311. Thus, programmable interconnect chip 311-1
2 interconnects electronic components (not shown) formed in
3 the upper left quadrant 300-1 of programmable PC board
4 300. Programmable interconnect chip 311-2 interconnects
5 electronic components (not shown) inserted into the
6 programmable PC board 300 in upper right quadrant 300-2.
7 Programmable interconnect chip 311-3 interconnects
8 electronic components (not shown) inserted into the
9 programmable PC board 300 in the lower right quadrant 300-3
10 and programmable interconnect chip 311-4 interconnects
11 electronic components (not shown) inserted into the lower
12 left quadrant 300-4 of programmable PC board 300. Thus the
13 structure of Figure 3b is capable of electrically
14 interconnecting the electronic components within each
15 quadrant not only among themselves but also to the
16 electronic components in other quadrants of the programmable
17 PC board 300. The structure of Figure 3b thus gives great
18 flexibility to the circuit designer in locating the
19 electrical components to perform a given system function.

20 Figure 3c illustrates a bus configuration wherein a
21 central bus 323-10 is formed on PC board 300 and
22 programmable interconnect chips 321-1, 321-2, 321-3, 321-4,
23 321-5 and 321-6 are connected by means of conductive busses
24 323-1, 323-2, 323-3, 323-4, 323-5 and 323-6, respectively,
25 to central conductive bus 323-10. Central bus 323-10 is
26 formed by placing conductive traces on printed circuit
27 board 300. Conductive busses 323-1 through 323-6 are
28 similarly formed by placing conductive traces on the PC
29 board. PC board 300 in general is a multilayer PC board
30 with two or more layers of conductive traces. The structure
31 shown in Figure 3c requires the traces making up bus 323-10
32 to be formed on one layer of PC board 300 and the traces
33 comprising conductive busses 323-1 through 323-6 to be
34 formed on a second layer. Electrical contact is then made
35 between selected ones of the traces comprising busses 323-1
36 through 323-6 to the traces comprising bus 323-10 by means
37 of holes, each hole electrically contacting the two or more
38 traces to be interconnected.

1 The structure of Figure 3c simplifies the
2 interconnections of the programmable interconnect chips
3 323-1 through 323-6 and improves the speed of inter-
4 connection of the common global bus signals but requires the
5 establishment of a protocol for use of bus 323-10. Bus
6 protocol is handled in a manner well known in the art by the
7 programmable interconnect chips 321-1 through 321-6.

8 An additional interconnect structure is shown in
9 Figure 3d. Here, programmable interconnect chips 331-1,
10 331-2, 331-3, 331-4, 331-5, 331-6 and 331-7 are
11 interconnected by means of busses 333-1, 333-2, 333-3,
12 333-5, 333-6 and 333-7 all of which emanate from or go to
13 central programmable interconnect chip 331-4. Chip 331-4 is
14 primarily or exclusively dedicated to interconnecting the
15 programmable interconnect chips 331-1 through 331-3 and
16 331-5 through 331-7. If desired and if the pins are
17 available on programmable interconnect chip 331-4,
18 programmable interconnect chip 331-4 also interconnects
19 electronic components mounted on the programmable PC board
20 particularly in the regions electrically adjacent to
21 programmable interconnect chip 331-4. Each of the
22 programmable interconnect chips 331-1 through 331-3 and
23 331-5 through 331-7 interconnects electronic components
24 mounted on the PC board in areas adjacent to the
25 programmable interconnect chip and has a certain number of
26 pins (depending upon the number of conductive paths in each
27 of busses 333-1 through 333-3 and 333-5 through 333-7)
28 dedicated to interconnecting itself, through PIC 331-4, to
29 other programmable interconnect chips 331. The advantage of
30 the structure in Figure 3d is that programmable interconnect
31 chip 331-4 can be configured to control the protocol for
32 communication between each of the other programmable
33 interconnect chips 331-1 to 331-3 and 331-5 to 331-7 and to
34 improve the speed of the random global interconnections
35 between the non-adjacent programmable interconnect chips.

36 Figure 4a illustrates a programmable printed circuit
37 board 400 of this invention containing a number of different
38 structures for both physically and electrically connecting

a 1 the electronic components to the programmable PC board
2 400. In the upper left hand corner of Figure 4a, an
3 electronic component is capable of being inserted into
4 sockets in the PC board such that leads on the component's
5 package electrically connect to and are physically retained
6 by ~~component~~ electrically conductive ^{component} holes (such as
7 component hole 402-1,1) in the PC board. The holes are
8 shown formed on a standard grid pattern such that one type
9 of programmable PC board can be used regardless of the
10 circuit function to be performed. This type of component
11 hole, called a socketed PCB configuration, allows the
12 electrically conductive pins on component packages to be
13 inserted into the component holes 402 in the PC board 400
14 and also to be removed from these component holes 402 (such
15 as hole 402-1,1) without destroying the package pins.

16 The lower left portion of PC board 400 has been
17 configured to contain electronic component packages which
18 are soldered into the programmable PC board 400. Typically,
19 component holes, such as hole 402-R,1, are also used in this
20 configuration and the holes can be placed in the board in
21 accordance with the pin configuration of the electronic
22 component packages to be mounted in the board. Thus one row
23 of holes (row R-1) is shown omitted from the PC board in the
24 lower left hand corner. The disadvantage of soldering
25 components to the PC board is that the components cannot be
26 easily removed. The advantage, of course, is greater
27 structural integrity, lower cost and higher reliability.
28 Soldered PC boards are commonly used in production to ensure
29 high reliability and quality and lower cost in the resulting
30 product.

31 The lower right hand corner of the PC board 400 in
32 Figure 4a comprises a solder pad configuration for the
33 mounting of electronic components on the programmable PC
34 board. As shown in Figure 4c, each pad, such as pad 402P-
35 R,C, is connected by an electrically conductive lead, such
36 as lead 407-R,C in Figure 4c to a component hole (such as
37 hole 402-R,C in Figure 4c) in the PC board to which a trace
38 (not shown in Figures 4a or 4c but the same as trace 103-R,C

1 shown in Figure 1a) is electrically attached for connecting
2 that component hole to a corresponding PIC hole (such as
3 hole 104-R,C in Figure 1b) connected to programmable
4 interconnect chip 405 on the programmable printed circuit
5 board. The solder pads can be formed on programmable PC
6 board 400 in accordance with the connection configuration of
7 the components to be mounted on the board, such as surface
8 mounted devices.

9
10 Figure 4b shows an end view of the structure shown in
11 top view in Figure 4a. Of importance, the socketed PC board
12 can use an adaptive socket 407 of a type commonly known in
13 the industry. For instance, appropriate sockets are
14 produced by Augat Interconnection Systems of 40 Perry
15 Avenue, Attleboro, Massachusetts 02703 and are disclosed in
16 Chapter 7 of revision 5.0 of their July 1987 Engineering
17 Design Guide.

18 Figure 5 illustrates a single programmable interconnect
19 chip 505 placed on the center of programmable PC board
20 500. Electronic components 506-1 through 506-4 are mounted
21 at various places on the programmable PC board 500 and are
22 interconnected by conductive traces, shown schematically as
23 503-1, 503-2, 503-3 and 503-4, to programmable interconnect
24 chip 505. Programmable interconnect chip 505, however, has
25 two busses extending from it to ports on the edge of the
26 printed circuit board. These ports comprise a test port 508
27 for the transmission of test signals from an external source
28 such as a computer to programmable interconnect chip 505 to
29 test the state of each conductive trace 503 coming into
30 programmable interconnect chip 505 and a control port 509
31 for allowing control signals from an external source such as
32 a computer to be transmitted to programmable interconnect
33 chip 505 to control the configuration of programmable
34 interconnect chip 505. The two ports 508 and 509 can be
35 actuated simultaneously such that the computer can determine
36 that the proper signals are present on selected traces
37 connected to PIC 505 during the configuring of PIC 505 and
38 during the operation of the system represented by FPPCB 500
and the attached electronic components 506-1 through 506-4

1 and PIC 505.

2 In general, the interconnection of one trace on the
3 programmable PC board to another trace can be carried out in
4 accordance with any one of a number of different
5 architectures. / Figures 6a and 6b illustrates a programmable
6 interconnect chip 605 in accordance with this invention
7 suitable for implementing the programmable interconnect
8 function in the structures described above. In Figure 6a
9 the programmable interconnect chip 605 contains a plurality
10 of cells 606-1,1 through 606-S,T where S represents the
11 number of rows of cells in the programmable interconnect
12 chip 605 and T represents the number of columns^{of} cells in
13 chip 605. Each cell has an array of electrically conductive
14 pads 607-1,1 through 607-M,N where M represents the number
15 of rows of pads in the cell and N represents the number of
16 columns of pads in the cell. Since each cell is identical
17 in configuration, only the conductive pads 607 associated
18 with cell 606-1,1 will be described in detail with the
19 understanding that the conductive pads associated with each
20 of the other cells 606-s,t (where s is an integer given by $1 \leq s \leq S$
21 and t is an integer given by $1 \leq t \leq T$) in chip 605
22 function identically.

23 Figure 6b illustrates the configuration of cell 606-1,1
24 and also of each of the other cells 606-s,t. In Figure 6b
25 horizontal conductive tracks 608-1 through 608-J (where J is
26 an integer representing the maximum number of horizontal
27 conductive tracks formed on programmable interconnect chip
28 605) are shown. In addition, vertical conductive tracks
29 609-1 through 609-K are shown where K is an integer
30 representing the maximum number of columns of conductive
31 tracks formed on programmable interconnect chip 605. The
32 horizontal conductive tracks 608-1 through 608-J are formed
33 on one level of interconnections on chip 605 while the
34 vertical conductive tracks 609-1 through 609-K are formed on
35 a second level of interconnections on chip 605. Typically,
36 these interconnections are formed in a manner well known in
37 the semiconductor processing arts and thus the method of
38 forming these interconnections will not be discussed. The

1 horizontal conductive leads 608-1 through 608-J have
2 differing lengths across the chip. The cell 606-1,1 shown
3 in the upper left hand corner of both Figure 6a and Figure
4 6b has a plurality of horizontal conductive leads 608
5 originating in and extending from cell 606-1,1 to each of
6 the other cells 606-1,2 through 606-1,T in the same row.
7 Likewise, cell 606-1,1 has a plurality of vertical
8 conductive leads 609 extending from cell 606-1,1X to each of
9 the other cells 606-2,1 to 606-S,1 in the same vertical
10 column.

11 The horizontal and vertical traces 608 and 609 have at
12 each of their intersections a programmable connective
13 structure such as for example, an antifuse. Typically, an
14 antifuse comprises a capacitive structure with a dielectric
15 capable of being broken down by the application of a
16 selected voltage to provide a conductive path between the
17 two plates of the capacitor. Antifuses are well known in
18 the art and thus will not be described in detail. Other
19 kinds of programmable elements can also be used depending
20 upon design considerations. The substrate of the
21 programmable interconnect chip 605 has formed in it selected
22 transistors to enable the programming of the antifuse
23 elements at selected intersections in accordance with design
24 requirements.

25 As shown in Figure 6b, vertical leads 609-1 through
26 609-K are formed on the programmable interconnect chip 605
27 so as to extend at a minimum across one cell 606 and at a
28 maximum across all cells. Thus a plurality of vertical
29 leads 609 cross each cell with the ^{lengths} ~~length~~ of leads varying
30 from being such as to extend across just that cell to being
31 such as to extend across all cells in a column.

32 Horizontal conductive leads 608-1 through 608-J
33 likewise extend across the programmable interconnect chip
34 605. Again, the horizontal leads 608 extending across one
35 cell vary in length such that they extend across only that
36 one cell up to a length which will extend across all
37 cells. In Figure 6b, breaklines are included to indicate
38 that the semiconductor chip 605 is only partially shown with

1 interior portions of the chip having been removed for
2 clarity. However, some conductive leads break not because
3 of the breaklines showing removal of semiconductor material
4 but rather because the conductive leads are intended to stop
5 at a given point. Small lines 618-1, 618-2 and 618-3 are
6 drawn at the terminal points of a conductive lead
7 perpendicular to that lead to indicate that the conductive
8 lead is intended to terminate at those points. A horizontal
9 conductive lead thus might comprise one conductive segment
10 each extending across the whole chip 605 or a plurality of
11 conductive segments extending across a section of the
12 chip. Similarly, the vertical conductive leads likewise
13 vary from one conductive lead which will extend across the
14 entire height of the chip or two or more conductive segments
15 each extending across a selected portion of the chip.

16 The particular configuration of the conductive leads
17 extending across one cell and from that cell to adjacent
18 cells depends upon an analysis of the electrical functions
19 to be carried out by the programmable printed circuit board
20 and is selected using the most probable types of system
21 requirements to be imposed on programmable interconnect chip
22 605. This selection depends upon an analysis of the circuit
23 functions to be performed by the programmable printed
24 circuit board of this invention and thus the actual
25 configuration of the programmable interconnect chip is
26 determined in light of the proposed uses for the
27 programmable printed circuit board.

28 To interconnect a given lead corresponding for example
29 to the lead 609-1 connected to pad A in cell 606-1,1 to a
30 given lead corresponding to a different pad either in cell
31 606-1,1 or in some different cell using the structure shown
32 in Figure 6b, an interconnection between the appropriate
33 vertical conductor 609 and the appropriate horizontal
34 conductor 608 is formed. For example, to connect pad A to
35 pad B (both in cell 606-1,1) the intersection of vertical
36 lead 609-1 and horizontal lead 608-1 is programmed by
37 applying a high voltage to this intersection in the circuit
38 so as to break down the dielectric between these two points

1 and form a conductive path therebetween. In addition, the
2 intersection of vertical conductor 609-4 and horizontal
3 conductor 608-1 is also subjected to a high voltage to break
4 down the insulation between these two leads to form an
5 additional conductive path between these two leads. Thus,
6 pad A is connected to pad B by conductors 609-1, 608-1 and
7 609-4. Should it be desired to connect pad A to any other
8 lead or pad then pad B will also be connected to that other
9 lead or pad. However, such a connection must be compatible
10 with the circuit in order to be made.

11 Figure 6b also illustrates the particular connections
12 which must be formed to connect pad A to pad D, pad A to pad
13 C or pad A to pad E. Should all of these connections be
14 made then pads B, D, C and E will also be connected to each
15 other through pad A.

16 Figure 6c illustrates a programmable interconnect chip
17 605 utilizing a single cross-point switch matrix array.
18 When the number of pads to be interconnected is quite small
19 (e.g., on the order of 100 to 300) then the structure of
20 Figure 6c has certain advantages of simplicity and ease of
21 fabrication. The structure shown in Figure 6c is simpler
22 than that shown in Figure 6b in that each pad (such as pad
23 A) is connected by a conductive trace (such as conductive
24 as lead 625-A) permanently to a vertical conductive lead (such
25 as lead 629-1. In addition, ^{the} vertical conductive lead ⁶²⁹⁻¹ is
26 permanently connected by via 624-1 (as shown by the solid
27 dot) to horizontal conductive line 628-1. Should it be
28 desired to connect pad A to any other pad accessible by a
29 vertical lead 629 passing over or under horizontal lead 628-
30 1, the circuit is programmed by applying a voltage at the
31 correct node (such as node 623-1) to form a conductive path
32 between ~~desired~~ ^{desired} vertical and the horizontal leads (such as
33 horizontal lead 628-1 and vertical lead 629-4) thereby to
34 connect pad A to pad B. Pad B is connected to vertical lead
35 629-4 by conductive trace 625-B. Note that each vertical
36 line is permanently connected to one horizontal line 628 by
37 a via (such as via 624-1). This greatly simplifies the
38 interconnection required to program the printed circuit

1 board of this invention since one pad can be connected to
2 another by only one programming element. However, as the
3 number of pads become large, this particular structure
4 becomes relatively inefficient in its use of space on the
5 programmable interconnect chip 605. The total number of
6 programming elements required equals the number of pads
7 squared.

8 Figure 6d shows a variation of the structure in Figure
9 6c. Using the structure of Figure 6d to interconnect pad A
10 (which connects to a PIC hole such as hole 104-1,1 shown in
11 Figure 1b) to pad D (which connects to a similar PIC hole
12 104) two programming elements must be programmed. Thus, the
13 element at the intersection of vertical lead 639-1 and
14 horizontal lead 638-1 must be programmed as must the element
15 at the intersection of vertical lead 639-(K-1) and
16 horizontal lead 638-1. However, as shown in the structure
17 of Figure 6d, each conductive pad such as pad A or pad D is
18 connected by means of a conductive trace such as trace 635-A
19 to a vertical lead 639. The number of horizontal ^{leads} ~~lead~~ is in
20 this embodiment, less than 1/2 the number of vertical leads
21 because ~~as~~ each horizontal lead connects two pads whereas
22 each vertical lead is connected directly to one pad only.
23 Thus, the structure ^{of Figure} 6d has greater flexibility than that
24 shown in Figure 6c at the price of two programming elements
25 per connection rather than one. The number of programming
26 elements is 1/2 the square of the number of pads. As the
27 number of pads become larger (for example above 200 to 500
28 pads) this structure becomes relatively inefficient.

29 Figure 6e illustrates the single switch cross-point
30 matrix array of Figure 6c with interconnections formed to
31 connect pad 1,1 to pad 4,1. To do this, the intersection of
32 the vertical lead $V_{1,1}$ and the horizontal lead H_1 is
33 programmed as is the intersection of the vertical lead $V_{4,1}$
34 and horizontal lead H_1 . Thus, two elements have been
35 programmed to connect pads 1,1 and 4,1. To connect pad 1,2
36 to pad 4,4, the programming elements at the intersection of
37 the vertical lead $V_{1,2}$ and the horizontal lead H_3 and of
38 the horizontal lead H_3 and the vertical lead $V_{4,4}$ are

a
1 programmed. Note that as a convention in Figure 6e,
2 wherever the intersection of a vertical and a horizontal
3 lead ~~are~~^{is} not shown to be electrically connected by a solid
4 dot, a programmable element (often shown by a hollow circle)
5 will be present even though a hollow circle is not shown at
6 such intersection.

u
7 Figure 7a shows in block diagram form the architecture
8 of the programmable interconnect chip 605. The interior
9 605a of chip 605 contains the cells 606 (as described in
10 conjunction with Figures 6a through 6e) and the horizontal
11 and vertical tracks 608 and 609 respectively. In peripheral
12 area 605b which forms an annular square around interior 605a
13 are placed control and programming circuits including shift
14 registers for selecting particular horizontal and vertical
15 tracks the intersections of which are to be programmed. In
16 addition, buffer circuitry for the test^{port} bus and the
17 control port bus ~~are~~^{is} provided in this region of chip 605.
18 Annular region 605c surrounds annular region 605b and
19 contains additional circuitry essential to the operation of
20 the chip such as mode selection circuitry which will
21 determine whether the programmable interconnect chip is in
22 the test mode, the operating mode or the programming mode.
23 Additional special circuitry as required will also be placed
24 in peripheral region 605c.

25 Figure 7b illustrates a programming structure and
26 particularly programming transistors and circuits to select
27 the intersection to be programmed of horizontal and vertical
28 conductive leads on the programmable interconnect chip using
29 only two transistors in the programming circuit path.
30 Utilization of the structure shown in Figure 7b allows the
31 programming current to reach into the hundreds of milliamps
32 to amperes range necessary to break down the dielectric
33 between the vertical and horizontal conductive leads to form
34 an interconnection therebetween with sufficiently low
35 resistance. For example, to program the intersection of
36 vertical conductive track V_1 and horizontal conductive track
37 H_1 , transistors Q1 and Q2 are provided. Transistor Q1 has
38 its gate connected to voltage source VGP_1 and transistor Q2

1 has its gate connected to a voltage source HGP_1 . The source
2 of transistor Q1 is connected to vertical conductive track
3 V1 while the drain of transistor Q1 is connected to
4 conductive lead VDP_1 . The source of transistor Q2 is
5 connected to horizontal lead H_1 and the drain of transistor
6 Q2 is connected to conductive lead HDP_1 . To program the
7 intersection of vertical lead V_1 and horizontal lead H_1 ,
8 VGP_1 is applied to take the gate of Q1 to a high voltage
9 V_{GH} , the gates of other transistors in the array such as
10 transistor Q3 ~~is~~^{are} held at zero volts and the drain voltage
11 VDP_1 on transistor Q1 is taken to V_{pp} . However, the gate
12 voltage of Q4 is taken high because HGP_1 is taken to a high
13 voltage to turn on transistor Q2. However, the voltage on
14 the drain of Q2 is taken to zero volts by driving HDP_1 to
15 zero and HDP_2 which applies^{a voltage} to the drain of Q4 is taken to
16 zero or to $V_{pp}/2$ ~~or to V_{pp} over-2~~ (which voltage is selected so as not
17 to program the programming element at the intersection of V_2
18 and H_2 . V_{pp} , the programming voltage, is typically 15 to 50
19 volts. V_{GH} , which is applied to lead VGP_1 , is larger than
20 V_{pp} by the transistor threshold voltage and thus is
21 approximately 18 to 53 volts. Because the devices Q1 to Q4
22 operate under high voltage, the threshold voltage of these
23 transistors is made approximately 3 volts. As a result of
24 the above-described voltages, only the programming element
25 at the intersection of conductive lead segments H_1 and V_1
26 will receive the full programming voltage V_{pp} and break
27 down.

28 Figure 7c shows a bidirectional amplifying circuit
29 capable of amplifying signals coming in either direction
30 depending upon control signals applied to the input and
31 output buffers contained within the circuitry. Thus, as
32 shown in Figure 7a, each pad on PIC 705 is connected to a
33 special function test line (illustrated in Figure 7c) and
34 the special function test line is then capable of being
35 connected to the test port by turning on the output buffer
36 through a high level signal applied to the lead labeled S on
37 the output buffer together with a high level enable signal
38 applied on the terminal labeled E. Simultaneously with the

1 application of a high level signal on the lead labeled S to
2 the output buffer, a low level signal is applied to the lead
3 labeled \bar{S} to the input buffer thereby turning off the input
4 buffer. Reverse polarity signals applied to terminals S and
5 \bar{S} result in the input buffer turning on and the output
6 buffer turning off thereby allowing a signal from the test
7 port to be applied to the pad. The S and E signals are
8 transferred to the peripheral circuits in annular region
9 ^{605b} of Figure 7a to select the pads on the PIC and the
10 ~~605b~~ leads of the components on the FPPCB to connect to the test
11 port.

12 Figures 8a and 8b illustrate structures for attaching
13 the program interconnect chip such as chip 105 in Figure 1a
14 to the PC board 100. Figure 8a illustrates a program
15 interconnect chip ^{which} contains pads with metal bumps shown in an
16 exploded view above the PIC holes (corresponding to holes
17 104-1,1 through 104-R,C shown in Figure 1b). A buffer
18 medium comprising an elastomeric material which under
19 pressure will conduct in the vertical direction but not the
20 horizontal direction, is shown placed between the program
21 interconnect chip and the PIC holes. The buffer medium
22 could also be a carrier using button springs of a type well
23 known in the art. This medium is a good buffer between the
24 surface of the PIC and FPPCB with their different surface
25 flatness and temperature coefficient. The particular
26 structure to be used to attach the programmable interconnect
27 chip to the programmable PC board will depend upon the
28 design requirements for the particular system utilizing the
29 combination of programmable PC board and programmable
30 interconnect chip and cost considerations.

31 Figure 8b ^{a4} shows an alternative structure for attaching
32 the programmable interconnect chip such as chip 105 in
33 Figure 1a directly to a programmable printed circuit board
34 such as board 100 in Figure 1a. In Figure 8b, the
35 programmable interconnect chip has formed on one surface
36 thereof a conductive pad to serve as an interface between a
37 conductive element on the chip and a metal bump consisting
38 of a soft solder such as lead tin placed on a nickel bottom

1 layer. Alternatively, the whole bump is made of indium. The
2 nickel is used to give strength to the bump. The
3 programmable PC board has solder formed in the PIC hole so
4 as to form a bump on the surface of the PC board to which
5 the programmable interconnect chip is to be attached. The
6 PIC hole such as hole 104-r,c in Figure 1b, is plated
7 typically with copper to a selected thickness such as 1
8 mil. The solder bump will, when the programmable
9 interconnect chip is brought into pressure contact with the
10 solder and the combined structure heated, form a solid
11 contact with the metal bump. The two materials will wet and
12 become one thus firmly securing and electrically connecting
13 the programmable interconnect chip to the programmable
14 printed circuit board. Solder bumps are well known in the
15 art and thus this structure will not be described in greater
16 detail. Other structures can be used to attach the
17 programmable interconnect chip such as chip 105 in Figure 1a
18 directly to a programmable printed circuit board such as
19 board 100 in Figure 1a. Such structures include attachment
20 of the PIC on the board and wire bonding of the pads on the
21 PIC to the PIC holes. Any other structure known in the art
22 to attach electronic components to a printed circuit board
23 can be used with this invention and the structures described
24 for this purpose are exemplary only.

25 In an alternative embodiment of this invention, a
26 printed circuit board comprises a first portion containing
27 conductive traces for interconnecting electronic components
28 formed thereon without the use of a programmable integrated
29 circuit and a second portion containing at least one
30 programmable integrated circuit for interconnecting .
31 electronic components formed on at least the second portion
32 of the printed circuit board. Electronic components formed
33 on the second portion of the printed circuit board are in
34 some cases interconnected with the electronic circuit formed
35 on the first portion of the printed circuit board by
36 conductive traces. These conductive traces typically will
37 run from the first portion of the printed circuit board to
38 at least one programmable integrated circuit for

1 interconnecting electronic components formed on the second
2 portion of the printed circuit board, thereby to
3 electrically connect the second portion of the printed
4 circuit board to the first portion of the printed
5 circuit board.

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